REMARKS

I. Introduction

In response to the Office Action dated August 24, 2005, Applicants respectfully submit that the specification as originally filed provides support for the amendment filed on June 9, 2005, and that claim 12 is patentable over the cited prior art, for the reasons set forth below. Applicants note with appreciation the allowance of claims 13-22.

II. The Objection To The Disclosure

The specification was objected to for failing to disclose the subject matter set forth in claim 12 (it was acknowledged that the drawings support claim 12). Applicants respectfully submit that the original disclosure does support claim 12 for the following reasons.

First, referring to page 7, lines 15-17 of the specification, the specification states: "In Fig. 1, a complementary PWM generation unit 1 generates complementary PWM signals not having a dead time yet, namely, a first PWM signal PWM1 and a second PWM signal PWM2 that is an inverted signal of the first PWM signal PWM1". The specification also states: "A dead time addition unit 2 adds dead times respectively to the first and second PWM signals PWM1 and PWM2 generated by the complementary PWM generation unit 1" (*see*, page 7, line 25 – page 8, line 2). As such, the specification explicitly discloses that the device of the present invention sets dead times in at least two PWM signals.

Furthermore, the specification states: "when the count value of the dead time timer 22 reaches the set value of the first dead time set register 24a (i.e., a set value of the first dead time), the upper phase signal SU rises and the first dead time t1 is set" (*see*, page 9, lines 1-4). As such, the specification explicitly discloses that the first dead time t1 is added to the positive edge of the

SU signal generated from the first PWM signal (which corresponds to the first edge of the first PWM signal).

The specification also states: "at this point, the dead time timer 22 restarts counting, and when its count value reaches the set value of the first dead time set register 24a (i.e., a set value of the second dead time), the lower phase signal SL rises and the second dead time t2 is set" (*see*, page 9, lines 7-9). As such, the specification explicitly discloses that the second dead time t2 is added to the positive edge of the SL signal generated from the second PWM (which corresponds to a second edge of the second PWM signal).

Finally, the specification states: "the first dead time to be added at the rise of the first PWM signal and the second dead time to be added at the rise of the second PWM signal can be individually set" (*see*, specification, page 9, lines 12-14). As such, the specification explicitly discloses that the second edge of the second PWM signal has the same direction of change (polarity) as that of the first edge of the first PWM signal.

Accordingly, in view of the foregoing explanation, which references the originally filed specification, it is respectfully submitted that claim 12 is supported by the original filed specification.

III. The Rejection Of Claim 12 Under 35 U.S.C. § 102

Claim 12 was rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 6,535,402 to Ying. Applicants respectfully submit that claim 12 is not anticipated by Ying for at least the following reasons.

As set forth in Applicants previous response, as recited by claim 12, the present invention relates to a device for controlling an inverter circuit which includes in part a dead time

calculating unit for calculating a first dead time and a second dead time, the first dead time being determined in response to a comparison between a count value of a timer and a first value stored in a register and the second dead time being determined in response to a comparison between a count value of a timer and a second value stored in a register. Claim 12 further recites a first dead time addition unit and a second dead time addition unit. As a result of this structure, the present invention can set the first or second dead time at an arbitrary value in response to the comparison between the count value of the timer and the first or the second value stored in the register. Consequently, the present invention advantageously sets the appropriate dead time in accordance with the characteristic of the inverter circuit so as to reduce the noise and the power consumption associated with the inverter circuit effectively.

As noted above, claim 12 explicitly recites that the first dead time is determined in response to a comparison between a count value of a timer and a first value stored in a register, and that the second dead time determined in response to a comparison between a count value of a timer and a second value stored in a register. In the pending rejection, col. 3, line 59 – col. 4, line 6 and col. 4, lines 35-46 of Ying are cited as disclosing this aspect of claim 12. However, upon review of Ying, it does not appear that any of these cited portions disclose the foregoing element recited by claim 12. *The cited sections of Ying merely state that the first dead time compensation signal is based in the pulse width modulation signal and that the second dead time compensation signal is based on a detected bias current crossing point* (*see*, Ying, col. 4, lines 35-47). Indeed, it appears that Ying is completely silent with regard to determining the alleged first dead time and second dead time based on any comparison, let alone doing so based on a timer and the value stored in a register. Thus, at a minimum, Ying fails to disclose or suggest the recited ***dead time calculating unit*** for calculating a first dead time and a second dead time, ***the***

first dead time determined in response to a comparison between a count value of a timer and a first value stored in a register and the second dead time determined in response to a comparison between a count value of a timer and a second value stored in a register.

It is further noted that Ying also appears silent with regard to individually compensating the dead times in each edge of the first and second PWM signals having the same polarity.

Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order for the prior art reference to anticipate the claim, and Ying, at a minimum, fails to disclose the dead time calculating unit, the first dead time addition unit and the second dead time addition unit, it is respectfully submitted that Ying does not anticipate claim 12.

For all of the foregoing reasons, it is respectfully submitted that claim 12 is patentable over the cited prior art.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: November 22, 2005